

WHAT IS CLAIMED IS:

1 1. A method of forming a semiconductor device comprising:
 2 providing a semiconductor substrate having a first region where a first
 3 oxide layer thickness is desired and a second region where a second oxide layer thickness
 4 is desired;
 5 introducing a halogen-containing impurities into said semiconductor
 6 substrate to form a higher halogen concentration in said first region than in said second
 7 region; and
 8 performing an oxidizing process on said semiconductor substrate to
 9 simultaneously form said first oxide layer thickness at said first region and said second
 10 oxide layer thickness at said second region.

1 2. The method of claim 1 further comprising the steps of:
 2 forming a first memory gate electrode on said second oxide layer
 3 thickness, said second oxide layer thickness formed on said semiconductor substrate in a
 4 memory region.

1 3. The method of claim 2 wherein said halogen-containing impurities
 2 introducing step comprises the step of: ^{an + 6.5 is}
 3 masking said (dielectric layer) to expose said first region; and
 4 wherein said halogen-containing impurities are introduced through said
 5 dielectric layer to said first region.

1 4. The method of claim 3 wherein said halogen-containing impurities
 2 introducing step comprises an ion implantation.

1 5. The method of claim 1 wherein said halogen-containing impurities
 2 introducing step comprises the step of introducing halogen-containing impurities into said
 3 first region and wherein said second region has substantially no halogen concentration
 4 therein.

1 6. The method of claim 1 wherein said halogen-containing impurities
 2 introducing step comprises the steps of introducing halogen-containing impurities into
 3 said first region at a first concentration and introducing halogen-containing impurities

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4 into said second region at a second concentration, said first concentration greater than
5 said second concentration.

1 7. The method of claim 5 wherein said halogen-containing impurities
2 introducing step comprises an ion implantation.

1 8. The method of claim 1 wherein said halogen-containing impurities
2 are selected from fluorine bearing impurities, chlorine bearing impurities, bromine
3 bearing impurities, and iodine bearing impurities.

1 9. The method of claim 1 wherein said semiconductor substrate also
2 includes a third region where a third oxide layer thickness is desired, and wherein said
3 halogen-containing impurities introducing step also introduces halogen-containing
4 impurities such that a different halogen concentration is formed in said third region than
5 in said first region or in said second region.

1 10. The method of claim 1 wherein said semiconductor device
2 comprises a flash EEPROM semiconductor device.

1 11. The method of claim 2 wherein said first memory gate electrode
2 comprises a floating gate electrode.

1 12. The method of claim 11 wherein said first memory gate electrode
2 is part of a stack gate cell.

1 13. The method of claim 11 wherein said first memory gate electrode
2 is part of a split gate cell.

1 14. The method of claim 2 wherein said first memory gate electrode
2 comprises a control gate electrode.

1 15. The method of claim 14 wherein said first memory gate electrode
2 is part of a stack gate cell.

1 16. The method of claim 14 wherein said first memory gate electrode
2 is part of a split gate cell.

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1 22. The method of claim 20 wherein said halogen containing
2 impurities are selected from fluorine bearing impurities, chlorine bearing impurities,
3 bromine bearing impurities, and iodine bearing impurities.

1 23 The method of claim 20 further comprising forming a third
2 thickness of dielectric material overlying a third region, said third region being spatially
3 apart from said first region and said second region.

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